CLAIMS

What is claimed is:

1. A bypass circuit for reducing plasma damage to a gate oxide of a metal-oxide semiconductor (MOS) wafer, the bypass circuit positioned on a semiconductor wafer, the semiconductor wafer comprising a substrate, the MOS transistor, a dielectric layer, and the bypass circuit, respectively, with the bypass circuit comprising:

a conductive wire comprising at least a first contact end and a second contact end, the first contact end electrically connecting with a gate electrode on the top of the MOS transistor, and the second contact end electrically connecting with a doped region in the substrate; and

a fusion area positioned in the conductive wire to disconnect the conductive wire and the MOS transistor;

wherein ions in the gate oxide are transmitted to the doped region via the conductive wire so as to reduce plasma damage to the gate oxide.

2. The bypass circuit of claim 1 wherein the conductive wire is composed of a plurality of contact plugs and a metal layer.

3. The bypass circuit of claim 1 wherein the conductive wire is a portion of a metal interconnect layer.

4. The bypass circuit of claim 1 wherein the fusion area is made of polysilicon.

4 5. The bypass circuit of claim 1 wherein the doped region is an n-well.

5 6. The bypass circuit of claim 1 wherein ions in the gate oxide are transmitted to the doped region via the conductive wire to neutralize the ions in the doped region so as to reduce plasma damage to the gate oxide.

7. A method for reducing plasma damage to a gate oxide of a metal-oxide semiconductor (MOS) wafer, the MOS transistor positioned on a substrate of a semiconductor wafer, the method comprising:

forming a dielectric layer covering the MOS transistor on the substrate;

etching the dielectric layer to form a first contact hole through to a surface of the MOS transistor, and to form a second contact hole through to a doped region in the substrate;

forming a bypass circuit on the dielectric layer and in the first and second contact hole, and a fusion area electrically connecting with the bypass circuit to electrically connect the MOS transistor and the doped region; and

disconnecting the fusion area after formation of the MOS transistor;

wherein ions in the gate oxide are transmitted to the doped region via the conductive wire so as to reduce plasma damage to the gate oxide.

8. The method of claim 7 wherein the bypass circuit is made of a metal layer.

9. The method of claim 7 wherein the bypass circuit is a portion of a metal interconnect layer.

10. The method of claim 7 wherein the fusion area is made of polysilicon.

11. The method of claim 7 wherein the doped region is an n-well.

12. The method of claim 7 wherein a thermal way is performed on the fusion area so as to cutoff the fusion area.

13. The method of claim 7 wherein a laser beam is used to irradiate the fusion area so as to cutoff the fusion area.

14. The method of claim 7 wherein ions in the gate oxide are transmitted to the doped region via the conductive wire to neutralize the ions in the doped region so as to reduce plasma damage to the gate oxide.